A Series of InGaP/InGaAs HBT Oscillators up to D-Band

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***Abstract*—In this paper, the development of a series of fixed-frequency heterojunction bipolar transistor (HBT) oscillators from the W- to D-bands is reported. The oscillators are designed based on feedback theory with a small-signal equivalent circuit. This design method enables the achievement of high-output-power oscillators for the management of the power that is generated at the current source inside the HBT. We use a 1 μm $\times$ 10 μm single-emitter InGaP/InGaAs HBT as an active device for each oscillator, and 50-Ω coplanar waveguides as transmission lines and resonators. Emitter output topology is adopted to reduce the chip size. The series of oscillators achieve the oscillation frequency of 74.8–146.7 GHz. To our knowledge, the 146.7-GHz fundamental oscillation frequency is the highest oscillation frequency achieved thus far using InGaP/InGaAs HBT technology. The output power of the 146.7-GHz oscillator is -18.4 dBm. The chip size of the oscillator is 731 μm $\times$ 411 μm.**

***Index Terms*—Coplanar waveguides, equivalent circuit, heterojunction bipolar transistors, indium compounds, millimeter-wave bipolar transistor oscillators.**

I. Introduction

MILLIMETER waves, in the frequency range of 30–300 GHz, are promising frequency resources. The number of millimeter-wave applications, such as wireless communication systems and radar systems, is rapidly increasing. Millimeter-wave oscillators are key components in achieving these systems. The desired requirements of the oscillators are high speed, high power, high reliability, low phase noise, and low cost. To satisfy these requirements, the selection of suitable device technology and the adoption of a suitable design method are indispensable.

High electron-mobility transistor (HEMT) millimeter-wave oscillators have been developed since the early 1990s [1], [2], because HEMTs achieve high unilateral gain (G_U). The highest reported oscillation frequency of an HEMT oscillator is 213 GHz [3]. However, the phase noise characteristics of HEMT oscillators are limited because of the high intrinsic flicker noise of HEMTs. DC and RF characteristics of HEMTs also vary easily, and it is difficult to maintain reproducibility.

The development of heterojunction bipolar transistor (HBT) millimeter-wave oscillators has been highly anticipated in recent years [4]–[6]. The speed of HBTs has been improved [7], [8] and the intrinsic flicker noise of HBTs is low. A push–push HBT oscillator oscillates at 108 GHz, and achieves the single-sideband (SSB) phase noise of -88 dBc/Hz at 1-MHz offset [9]. The SSB phase-noise value is 20 dB lower than that of HEMT oscillators around that frequency [10]. DC and RF characteristics of HBTs also show excellent reproducibility in comparison to those of HEMTs. We have chosen to study the InGaP/InGaAs HBT, which is more reliable than the AlGaAs/GaAs HBT. In addition, the InGaP/InGaAs HBT shows higher breakdown voltage, and lower manufacturing cost than InP-based HBTs.

Almost all oscillators in the microwave band and millimeter-wave band are designed by methods based on negative resistance theory [2], [5], [6], [9]. The design methods enable the simulation with raw s-parameters, which are measured using network analyzers. However, the magnitude of negative resistance is not necessarily related to the magnitude of output power, and it is difficult to determine a design plan for high-output-power oscillators. We developed a design method based on feedback theory with a small-signal equivalent circuit of an HBT. The method enables the management of the power, which is generated at the current source inside the HBT. Almost all generated power, except that which is needed for the continuance of oscillation, is collected from an output port. Since the method uses an equivalent circuit, it also enables the design of an oscillator oscillating at above 110 GHz, which is the frequency limit of commercialized network analyzers. Using the design method, we analyze three topologies: collector output, base output, and emitter output. We select the emitter output topology from among them because it represents the highest output power with the smallest chip size. After the small-signal simulation, we also perform a harmonic-balance simulation with a large-signal equivalent circuit to reconfirm the oscillation and to evaluate the absolute oscillation power.

In this paper, the InGaP/InGaAs HBT technology is described in Section II. A small-signal equivalent circuit and a large-signal equivalent circuit of the HBT are presented in Section III, and the models of coplanar waveguides (CPWs) are introduced in Section IV. The oscillator circuit design method is explained in Section V, and the measured results are presented in Section VI.

II. InGaP/InGaAs HBT Technology

InGaP/InGaAs HBT oscillators are fabricated on a 635-μm-thick 4-in semi-insulating GaAs wafer. Fig. 1 shows a cross-sectional view of the InGaP/InGaAs HBT technology. Both epitaxy and photolithography are performed in our laboratory. The graded InGaAs base layer realizes high-speed performance.

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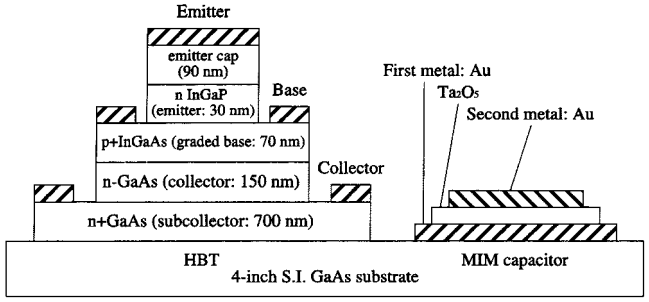

Fig. 1. Cross section of the InGaP/InGaAs HBT technology.

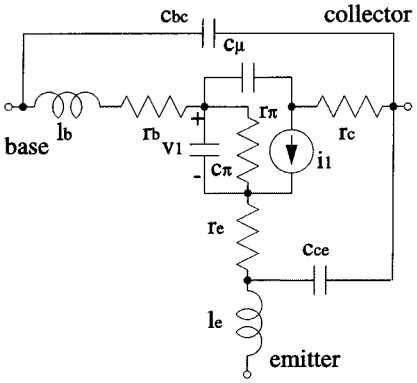

Fig. 2. Small-signal equivalent circuit.

A 1 μm $\times$ 10 μm single-emitter HBT occupies an area of 20 μm $\times$ 20 μm. The breakdown voltage BV_{CBO} is 7.8 V, and BV_{CEO} is 8.4 V. A reliability test has not been performed for this HBT, however, other HBTs, the emitter–base structure of which are the same as that of the present HBT, have withstood a 1000-h reliability test with a current density (J_C) of 50 kA/cm^2, an ambient temperature (T_a) of 125 °C, and a collector–emitter voltage ($V_{\rm CE}$) of 3.5-V references.

This technology also provides Ta_2O_5 metal–insulator–metal (MIM) capacitors of 0.93 fF/μm^2.

Devices are wired by two 1-μm-thick gold layers with a 2-μm-thick polyimide insulating layer.

III. Equivalent Circuits of the HBT

A small-signal equivalent circuit and a large-signal equivalent circuit are employed in the oscillator design. The oscillation condition is analyzed using the small-signal equivalent circuit. The absolute output power is evaluated by a harmonic-balance simulation using the large-signal equivalent circuit. We use an HP 85150B microwave design system (MDS) as the circuit simulator.

Fig. 2 shows the small-signal equivalent circuit. Table I lists the values of the circuit parameters. Considering the reliability, we extracted the circuit parameters and fabricated oscillators from the measured s-parameters under the bias condition of the collector–current $I_C = 5$ mA and the collector–emitter voltage $V_{\rm CE} = 2.5$ V. However, it became clear during the measurement that the oscillators exhibit excellent performance under the high collector–current bias conditions of around $I_C = 20$ mA. Table I also lists the circuit parameters of $I_C = 18$ mA and $V_{\rm CE} = 1.7$ V to enable comparison with the measured results.

TABLE I
Small-Signal Equivalent-Circuit Parameters

Bias	Ic = 5 mA Vce = 2.5 V	Ic = 18 mA Vce = 1.7 V	Bias	Ic = 5 mA Vce = 2.5 V	Ic = 18 mA Vce = 1.7 V
r_b	14.9 Ω	11.2 Ω	c_μ	13.7 fF	7.0 fF
r_π	136 Ω	24.0 Ω	c_{bc}	9.16 fF	17.5 fF
r_c	16.0 Ω	77.8 Ω	c_{ce}	9.50 fF	11.5 fF
r_e	4.25 Ω	4.78 Ω	l_b	10.2 pH	2.22 pH
c_π	349 fF	652 fF	l_e	17.0 pH	17.8 pH

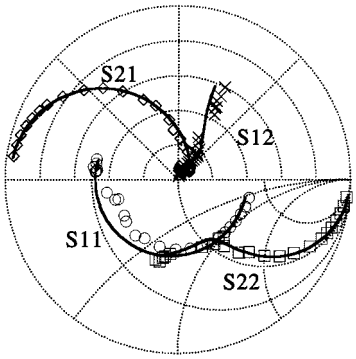

Fig. 3. S-parameters of $I_C = 18$ mA and $V_{\rm CE} = 1.7$ V. Markers: measured, lines: simulated, full scale of S_{11} and S_{22} is 1.0, full scale of S_{21} is 10.0, and full scale of S_{12} is 0.5.

The test element of the HBT is a common emitter type. Through-reflect-match (TRM) calibration is performed on the GaAs substrate using calibration standards of our own making. The s-parameters are measured by an HP 85109C vector network analyzer (VNA) and a pair of HP 85104A millimeter-wave test sets in two bands: 1–50 and 75–110 GHz (W-band). The s-parameter measurement in the 50–75-GHz band (V-band) is impossible because of the parasitic oscillation due to the poor reflection characteristics of the V-band probes. Fig. 3 shows the s-parameter plots of measured results under the bias condition of $I_C = 18$ mA, and $V_{\rm CE} = 1.7$ V and simulated results. The full scales for S_{11} and S_{22} are 1.0, and the full scales for S_{21} and $S12$ are 10.0 and 0.5, respectively. The simulated results almost agree with the measured results in the wide band, and we believe that the small-signal equivalent circuit operates satisfactorily in the lower range of the D-band, i.e., 110–170 GHz.

Fig. 4 shows h_{21} and G_U, which are converted from the measured s-parameter results shown in Fig. 3. The magnitude of S_{21} shows the maximum value at the bias point; however, f_T and $f_{\rm max}$ do not necessarily attain the maximum values. Although the value of $f_{\rm max}$ is estimated from G_U to be 170 GHz, we believe that $f_{\rm max}$ becomes higher after the following improvements: removing the influence of parasitic elements originating from the layout pattern of the test element and adjusting the bias condition to the optimum point. The value of f_T is difficult to estimate because the slope of h_{21} becomes gentle in the W-band. This phenomenon is also caused by the parasitic elements.

The large-signal equivalent circuit is a Gummel–Poon model connected by parasitic capacitors and inductors, as shown in

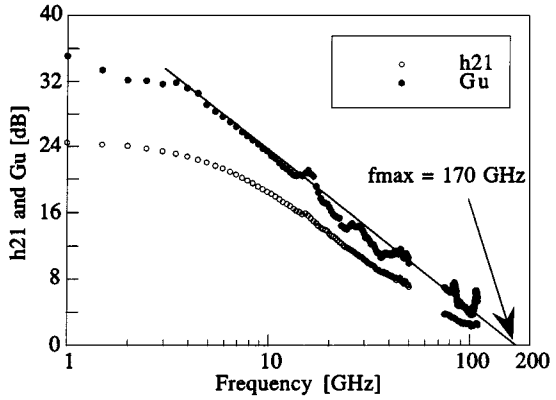

Fig. 4. Performance of HBT.

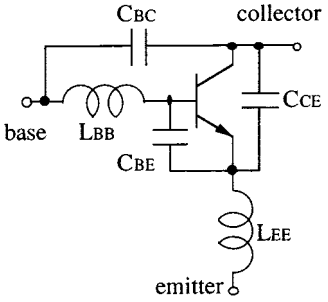

Fig. 5. Large-signal equivalent circuit.

TABLE II
LARGE-SIGNAL EQUIVALENT-CIRCUIT PARAMETERS

BF	40.0	CJC	15.0E-15	RE	3.30
ISE	17.0E-18	VJC	1.15	RC	16.0
NE	1.70	MJC	0.50		
N	1.00	XCJC	1.00	CBC	12.0 fF
TF	980E-15	CJE	76.0E-15	CBE	22.0 fF
BR	9.70E-3	VJE	1.40	CCE	7.70 fF
EG	1.42	MJE	0.50	LBB	18.0 pH
IS	400E-27	RB	21.0	LEE	16.0 pH

Fig. 5. For parameter extraction, Gummel plots, I–V characteristics, and the above-mentioned s-parameters are used. Table II shows the values of the large-signal equivalent-circuit parameters.

The Gummel plot data, i.e., I_C and I_B, are measured under the following conditions: $V_{\rm CE}$ and $V_{\rm BE}$ are kept at the same voltage and the voltage is swept in the range of 1.02–1.38 V. The I–V characteristic parameter, i.e., I_C, is measured under the condition that I_B is increased by 120 μA, and $V_{\rm CE}$ is swept in the range of 0.0–3.0 V.

Figs. 6 and 7 show the measured and simulated results of Gummel plots and I–V characteristics, respectively. The accuracy of the simulation is sufficient for the oscillator design. The average dc gain (β) is 17 with a turn-on $V_{\rm BE}$ of 1.4 V at the operating current density.

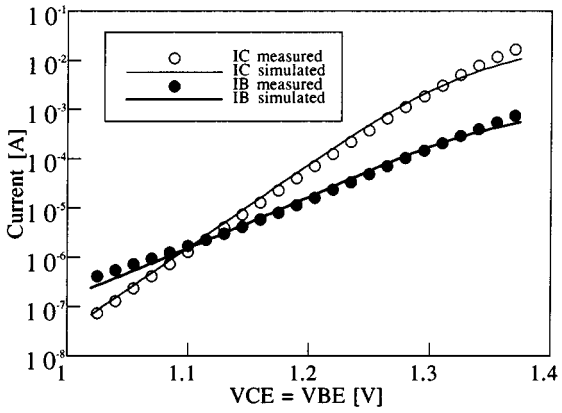

Fig. 6. Gummel plot.

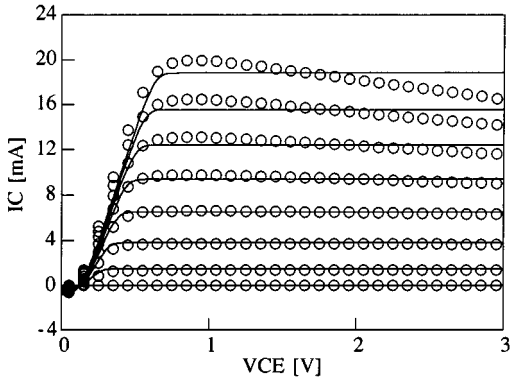

Fig. 7. I–V characteristics. Circles: measured, lines: simulated ($\Delta I_B = 120$ μA).

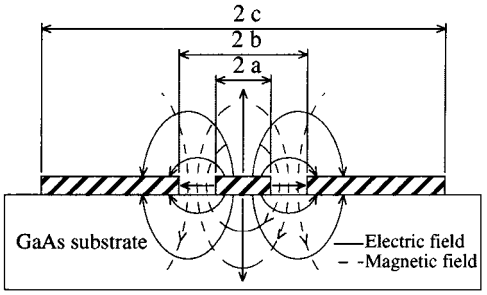

Fig. 8. Cross section of CPW with electric- and magnetic-field distributions.

IV. CPW MODELS

We use CPWs as transmission lines because they can easily be used to wire the devices and they are fabricated by a simple process. Fig. 8 shows a cross-sectional view of a CPW. In oscillators, the dimensions of CPWs are usually $2a = 30$ μm, $2b = 70$ μm, and $2c \geq 370$ μm. The characteristic impedance Z_0 is 50 Ω. However, test elements of this size were not available when the oscillators were designed, and the model parameters were estimated from the measured result of test elements twice the size, namely, $2a = 60$ μm, $2b = 140$ μm, and $2c = 640$ μm.

We measured the test elements of the CPWs in the W-band, and prepared three types of CPW models: a straight-line model, a fringe model of a short stub, and a T-junction model. The

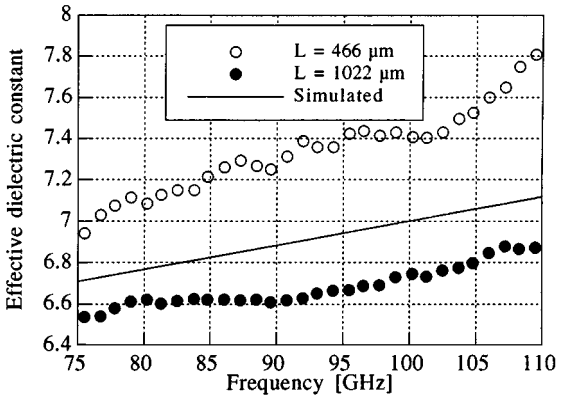

Fig. 9. Effective dielectric constant in W-band.

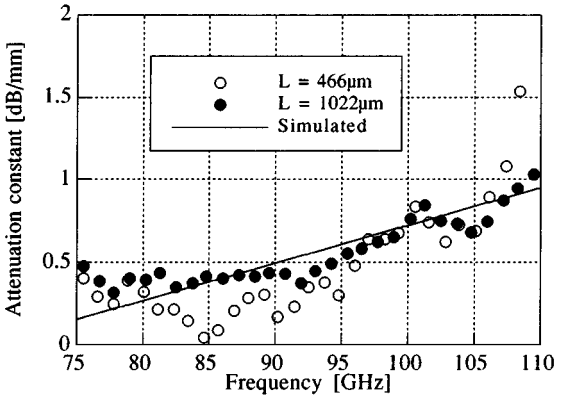

Fig. 10. Attenuation constant in W-band.

straight-line model is characterized by four parameters: characteristic impedance Z_0, physical length L, effective dielectric constant $\varepsilon_{r\text{eff}}$, and attenuation constant α, as shown in (1)–(4). The effective dielectric and attenuation constants are easily varied by factors such as the test element shape and manner of probe contact. We measured two lengths of CPWs, i.e., 466 and 1022 μm, and estimated linear approximate equations, considering the proportional weight of the line length. Figs. 9 and 10 show the measured and simulated results of the effective dielectric and attenuation constants, respectively. The equation of the attenuation constant is not directly incorporated in the simulation, and it is exchanged with the equation of the parasitic series resistance shown by (5) as follows:

$$Z_0\ [\Omega] = 50 \tag{1}$$

$$L\ [\mu\text{m}] = (\text{Physical line length}) \tag{2}$$

$$\varepsilon_{r\text{eff}} = 0.0115 \cdot f\ [\text{GHz}] + 5.85 \tag{3}$$

$$\alpha\ [\text{dB/mm}] = 0.0227 \cdot f\ [\text{GHz}] - 1.54 \tag{4}$$

$$r_S\ [\Omega/\text{mm}] = \frac{2 \cdot Z_0\ [\Omega] \cdot \alpha\ [\text{dB/mm}]}{20 \cdot \log_{10} e} = 0.261 \cdot f\ [\text{GHz}] - 17.7. \tag{5}$$

The fringe model of the short stub is represented by a straight line of $L_s = 0.51b$ and a shunt resistor of 1.3 Ω, as shown in Fig. 11(a).

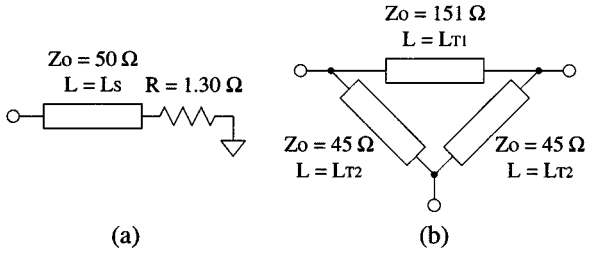

Fig. 11. (a) Fringe model of short stub. (b) T-junction model.

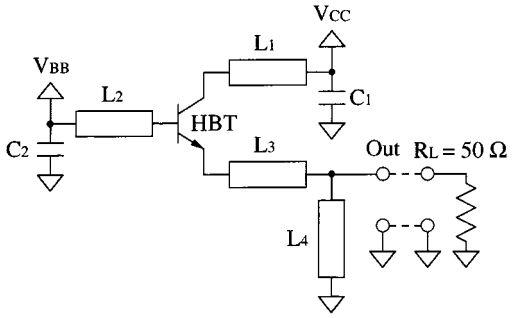

Fig. 12. Schematic circuit diagram.

The T-junction model is expressed not by the star network, but by the delta network, as shown in Fig. 11(b), because the transmitted energy trough of a CPW is mainly concentrated in the gap between the center conductance and ground pattern. The energy current of radio waves is equal to the vector product of the electric and magnetic fields, and the area of high-energy current density in the CPW is around the gap area, as shown in Fig. 8. The parameter values of the T-junction are $L_{T1} = 1.97b$ and $L_{T2} = 1.25b$. In the layout of the T-junction, ground patterns are wired by the second gold layer of 4 μm to maintain the same potential.

V. Oscillator Design

Fig. 12 shows a schematic diagram of an oscillator circuit. Elements L_1–L_4 represent CPWs with $Z_0 = 50\ \Omega$. The characteristics of the oscillators are adjusted by varying these CPW lengths. The bias voltage is supplied from the short stubs L_1, L_2, and L_4 for layout convenience. The resistor R_L is a 50-Ω load.

In the first step of designing an oscillator, the HBT is exchanged for the small equivalent circuit, and CPWs are also exchanged for proper CPW models. Fig. 13 shows the gain block diagram of the exchanged circuit.

The next step is to evaluate the oscillation condition. The voltage-controlled-current source i_1 is regarded to be independent, and an alternating current is supplied to i_1. In the gain block diagram, this means that the loop is cut at i_1. The current i_1 generates intrinsic base–emitter voltage v_1 via a transimpedance Z_{loop}. The voltage v_1 is calculated by small-signal simulation because the equation is complex. The voltage v_1 generates the new current $i_{1\text{new}}$ via feedback transconductance g_m. The loop gain G_{loop} is determined as the ratio of $i_{1\text{new}}$ to i_1.

The oscillation condition consists of the magnitude and phase conditions. The magnitude condition is selected to be 3 dB with

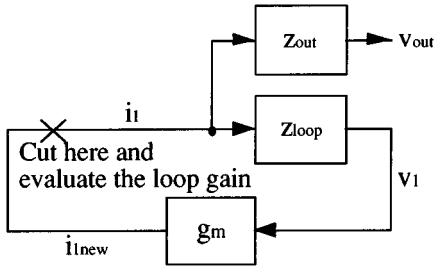

Fig. 13. Gain block diagram.

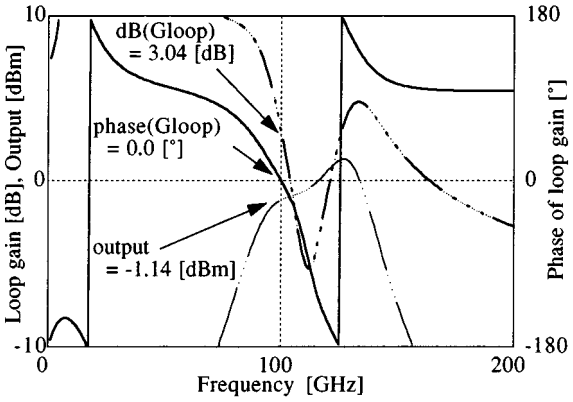

Fig. 14. Example of oscillator design.

a margin. The phase condition is 0.0°. Equations (6)–(8) express the oscillation condition as follows:

$$G_{\rm loop} = \frac{i_{1\rm new}}{i_1} = z_{\rm loop} \cdot g_m = \frac{v_1}{i_1} \cdot \frac{q \cdot I_{C(\rm DC)}}{k \cdot T} \quad (6)$$

$$\mathrm{dB}(G_{\rm loop}) \geq 3.0\,[\mathrm{dB}] \quad (7)$$

$$\mathrm{phase}(G_{\rm loop}) = 0.0[^\circ] \quad (8)$$

$I_{C(\rm DC)}$ is the collector direct current, $k \approx 1.38 \times 10^{-23}$ J/K, $T \approx 300$K, and $q \approx 1.60 \times 10^{-19} C$.

While the oscillation condition is being evaluated, an output voltage $V_{\rm out}$, which is generated by the independent current i_1, is optimized to the maximum value. Owing to the optimization, the undesirable power consumption at the parasitic resistors is minimized and the power efficiency becomes high. This is the greatest merit of our design method. In the conservative design method of negative resistance, it is impossible to optimize the output power.

The following is an example of oscillator design at 100 GHz. As the magnitude margin of 3 dB is not satisfied by the small-signal equivalent-circuit parameters of $I_C = 5$ mA and $V_{\rm CE} = 2.5$ V, we adjust the only the $I_{C(\rm DC)}$ value to 12 mA. The magnitude of $G_{\rm loop}$ is increased proportionally to $I_{C(\rm DC)}$, as shown by (6). The alternating current amplitude i_1 is assumed to be the collector direct current $I_{C(\rm DC)}$.

Fig. 14 shows the loop gain and magnitude of $V_{\rm out}$. At the target frequency of 100 GHz, the magnitude of $G_{\rm loop}$ is 3.04 dB and the phase of $G_{\rm loop}$ is 0.0°. No undesirable oscillation occurs because no frequency satisfies the oscillation condition without 100 GHz. The magnitude of $V_{\rm out}$ is optimized to -1.14 dBm.

Incidentally, HBTs are three-port elements, and the following three types of circuit topologies are considered:

TABLE III
OSCILLATOR DESIGN PARAMETERS

Designed frequency [GHz]	70	80	90	100	110	120
I_C [mA]	5.0	6.5	9.0	12.0	15.5	20.0
L_1 [μm]	103.8	128.4	96.8	79.3	65.9	50.1
L_2 [μm]	156.2	81.2	60.9	43.3	32.0	28.8
L_3 [μm]	405.0	354.3	315.0	283.5	257.7	236.2
L_4 [μm]	29.6	25.9	37.1	34.7	24.7	14.5

1) collector output;
2) base output;
3) emitter output.

We select emitter output topology from among them for the following two reasons.

First, the output power is evaluated to be maximum in our design method. The order of output power is emitter output topology followed by collector output topology and base output topology. However, the difference between the first two topologies is small.

Second, the chip size of emitter output topology is minimum. A small chip size is advantageous for low manufacturing cost. To satisfy the oscillation condition, inductance is needed for the collector and base, and capacitance is needed for the emitter. An inductance is realized with a short stub shorter than $\lambda/4$. The capacitance requires a short stub longer than $\lambda/4$, however, extra layout area is not needed for achieving capacitance when the impedance exchange layout is considered against the load resistance. The chip size of emitter output topology becomes the smallest for this reason. In our layout rule, the chip size of emitter output topology is 30% smaller than that of collector output topology.

The absolute output power is evaluated by a harmonic-balance simulation using the large-signal equivalent circuit to ensure accuracy. Although the harmonic-balance simulation enables further output power optimization using the results of small-signal analysis as the initial value, we decided not to utilize this method this time.

Table III lists the design parameters for every 10 GHz. Fig. 15 shows a micrograph of the oscillator designed at 120 GHz. The chip size is 731 μm $\times$ 411 μm. The bias voltage is supplied from the left-hand side, and the RF signal is output from the right-hand side. The CPW is tapered to $2b = 140$ μm at the output port to fit the 100-μm probe pitch width.

VI. MEASUREMENT RESULTS

The oscillators are measured by on-wafer probing. The RF output signal is sensed by a probe, and transferred to a harmonic mixer through waveguides. We use two mixers: HP 11970W for the W-band measurements and Farran WHMP-06 for the D-band measurements. The signal is down-converted by one of these mixers, and the IF signal is measured using the spectrum analyzer HP 71209A.

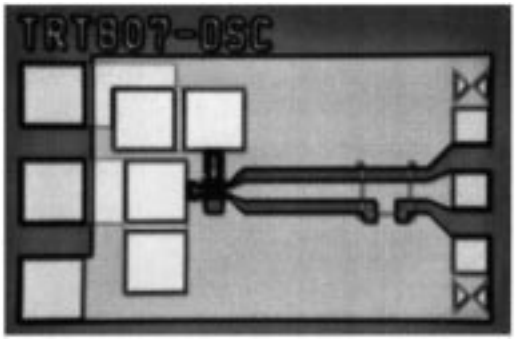

Fig. 15. Micrograph of oscillator (731 μm $\times$ 411 μm).

TABLE IV
REPRESENTATIVE MEASURED RESULTS

Designed frequency [GHz]	70	80	90	100	110	120
Oscillation frequency [GHz]	74.8	91.3	104.4	118.4	134.2	146.7
Output [dBm]	-0.6	-1.7	-3.4	-8.1	-10.4	-18.4
SSB phase noise [dBc/Hz @ 1MHz]	-97	-89	-95	-83	-72	-65
I_C [mA]	24.4	6.7	22.5	21.0	12.1	13.4
V_{CE} [V]	5.3	2.5	3.0	2.5	2.7	2.0

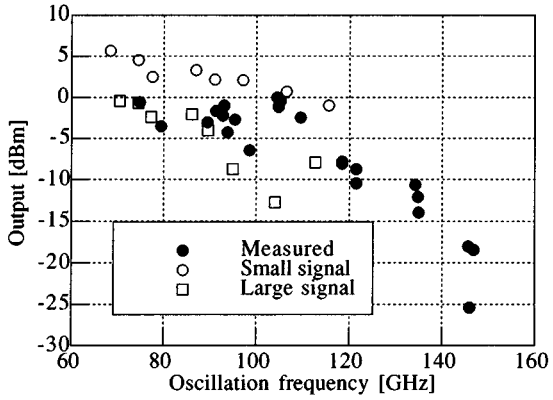

Fig. 16. Oscillation frequency and output power.

The probe insertion loss is measured in the W-band by the VNA. The values are, e.g., 1.03 dB at 75 GHz and 1.28 dB at 110 GHz. The upper limit frequency of the VNA is 110 GHz, and the insertion loss is regarded to be uniformly 1.0 dB in the D-band. For harmonic mixers, we use the catalog values for the insertion loss.

Table IV summarizes the representative measured results. Fig. 16 shows the relationship between oscillation frequency and output power of the measured and simulated results. The simulated results consist of the small-signal analysis results and the large-signal analysis results. In the small-signal analysis, the circuit parameter of $I_C = 18$ mA and $V_{\rm CE} = 1.7$ V are used. Although small-signal analysis yields favorable results and large-signal analysis yields unfavorable results, the trends

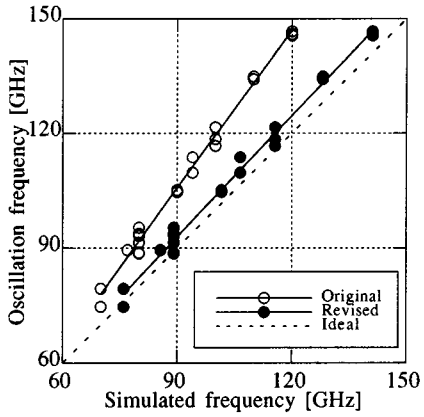

Fig. 17. Simulated frequency and oscillation frequency.

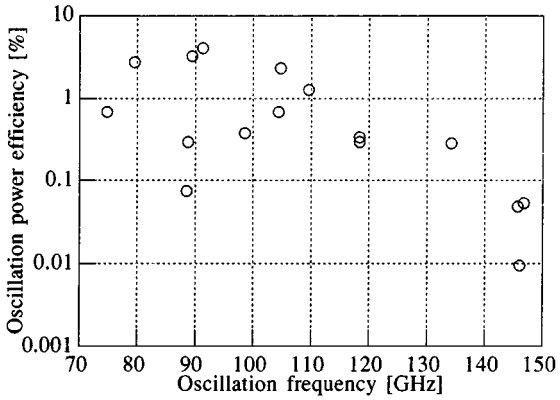

Fig. 18. Power efficiency of oscillators.

of both analyses are almost the same as those of the measured results.

The relationship between design frequency and oscillation frequency is represented by the white circles in Fig. 17. Although the plots show a linear tendency, the maximum difference is 26.7 GHz. We consider that such a difference is caused by estimation errors of the base–collector capacitance $c_{\rm bc}$ and the effective dielectric constant $\varepsilon_{r\rm eff}$. On the basis of the measurement results of other test elements, we are convinced that the effective $c_{\rm bc}$ value, which depends on the layout pattern, of the test element for equivalent-circuit parameter extraction is about 9.0 fF greater than that of the oscillators. On the other hand, $\varepsilon_{r\rm eff}$ is estimated as (9) from the latest measured result of the CPW test element of $2a = 30$ μm, $2b = 70$ μm, and $L = 1210$ μm. The difference between (3) and (9) is caused by the influence of the surface wave, which becomes conspicuous as the scale of CPW enlarges. The thickness of the GaAs substrate is 635 μm, and the cutoff frequency for the $\rm TE_0$ surface-wave mode is about 35 GHz [11]. Usual slope values for approximate equations of $\varepsilon_{r\rm eff}$ are positive, and the small negative slope value of (9) is caused by measurement errors. The line-length parameters of the short-stub model and the T-junction model for $2b = 70$ μm are also extracted to $L_S = 0.30b$, $L_{T1} = 1.75b$, and $L_{T2} = 1.57b$. The black circles in Fig. 17 represent the simulation result obtained with the revised $I_C = 18$ mA and $V_{\rm CE} = 1.7$ V small-signal circuit parameters of

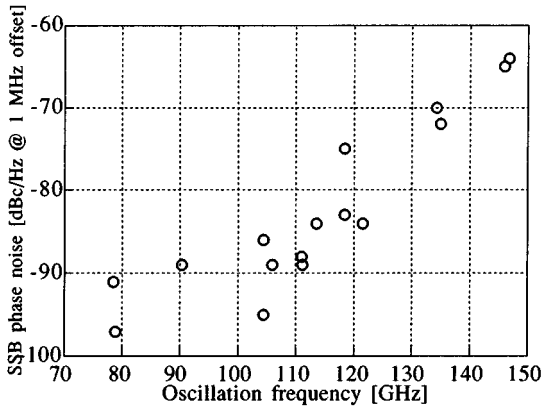

Fig. 19. Oscillation frequency and SSB phase noise.

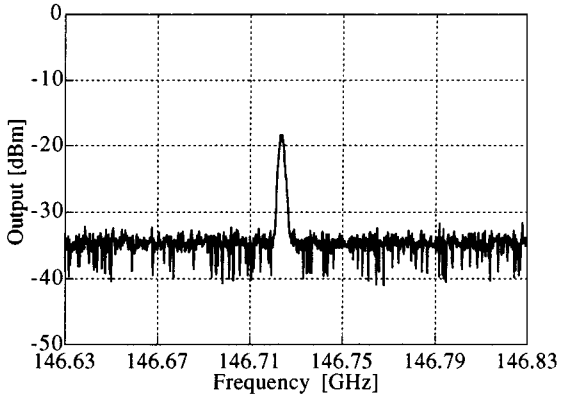

Fig. 20. 146.7-GHz oscillation spectrum. $RBW = 2.15$ MHz, $VBW = 100$ kHz, 51.9-dB measurement loss is corrected.

$c_{\rm bc} = 8.5$ fF and CPW models of $2b = 70$ μm. This simulation result shows good agreement with the measured result

$$\varepsilon_{\rm reff} = -0.00159 \cdot f\ [\rm GHz] + 6.57. \tag{9}$$

Fig. 18 shows the measured results of the oscillation power efficiency, which is the ratio of output RF power to input dc power. The efficiency decreases drastically as the frequency increases. This is because the power generated by the HBT is mainly used for the continuance of oscillation as the oscillation frequency approaches $f_{\max}$. The efficiency at 110 GHz is 1%.

Fig. 19 shows the measured results of oscillation frequency and SSB phase noise. The SSB phase noise is also measured using the spectrum analyzer. All noise values are converted to the value at 1-MHz offset. We believe that our oscillators achieve an optimum performance level.

In the measured results, the highest oscillation frequency is 146.7 GHz. To our knowledge, this is the highest oscillation frequency achieved using the InGaP/InGaAs HBT process. The spectrum is shown in Fig. 20. The output power is -18.4 dBm with a converted SSB phase noise value of -65 dBc/Hz at 1-MHz offset.

VII. Conclusion

In this paper, we have described the design method and measured performance of a series of HBT oscillators in the W- and D-bands. We selected the InGaP/InGaAs HBT, which exhibits high reliability and low flicker noise. The design method based on the feedback theory and emitter output topology enable the achievement of oscillators with high output power, low SSB phase noise, and small chip size. To our knowledge, the oscillator with 146.7-GHz oscillation frequency is the highest frequency fundamental-mode oscillator using InGaP/InGaAs HBT technology ever reported.

Our next objectives are the development of oscillators with higher oscillation frequency and higher output power. To achieve higher oscillation frequency, we must improve the speed of the HBT. To realize higher output power, we must improve the precision of equivalent circuits, optimize the bias condition, and develop the combined power topology of multiple oscillators.

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